

FIG. 1
(PRIOR ART)

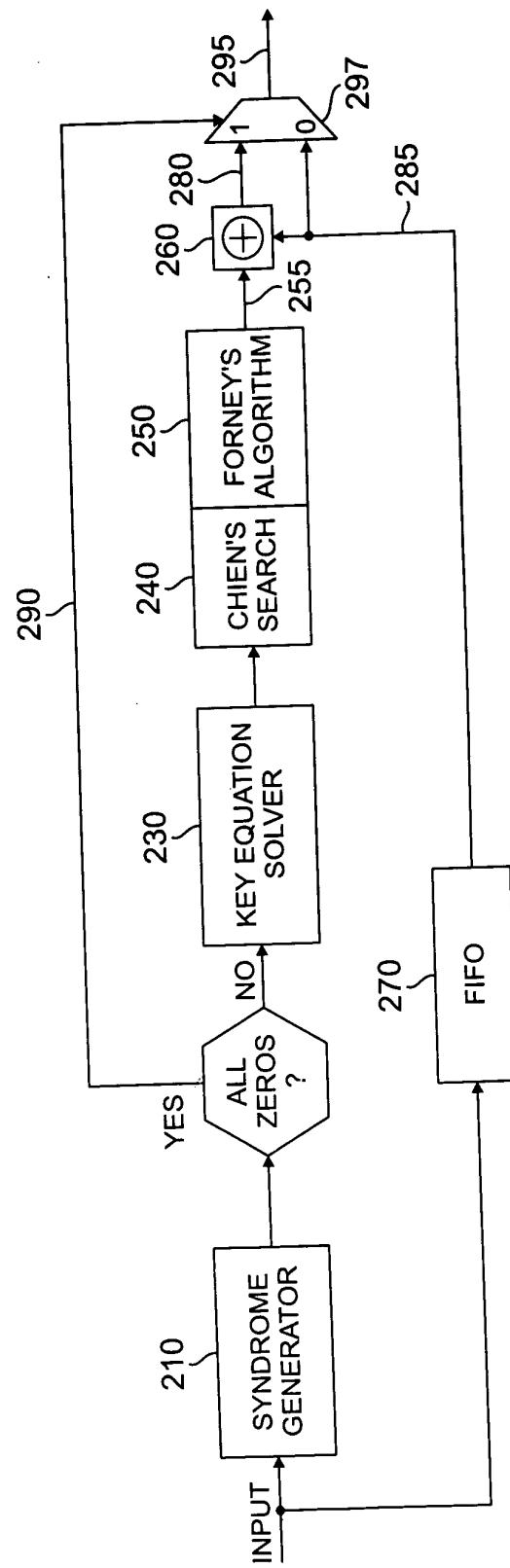
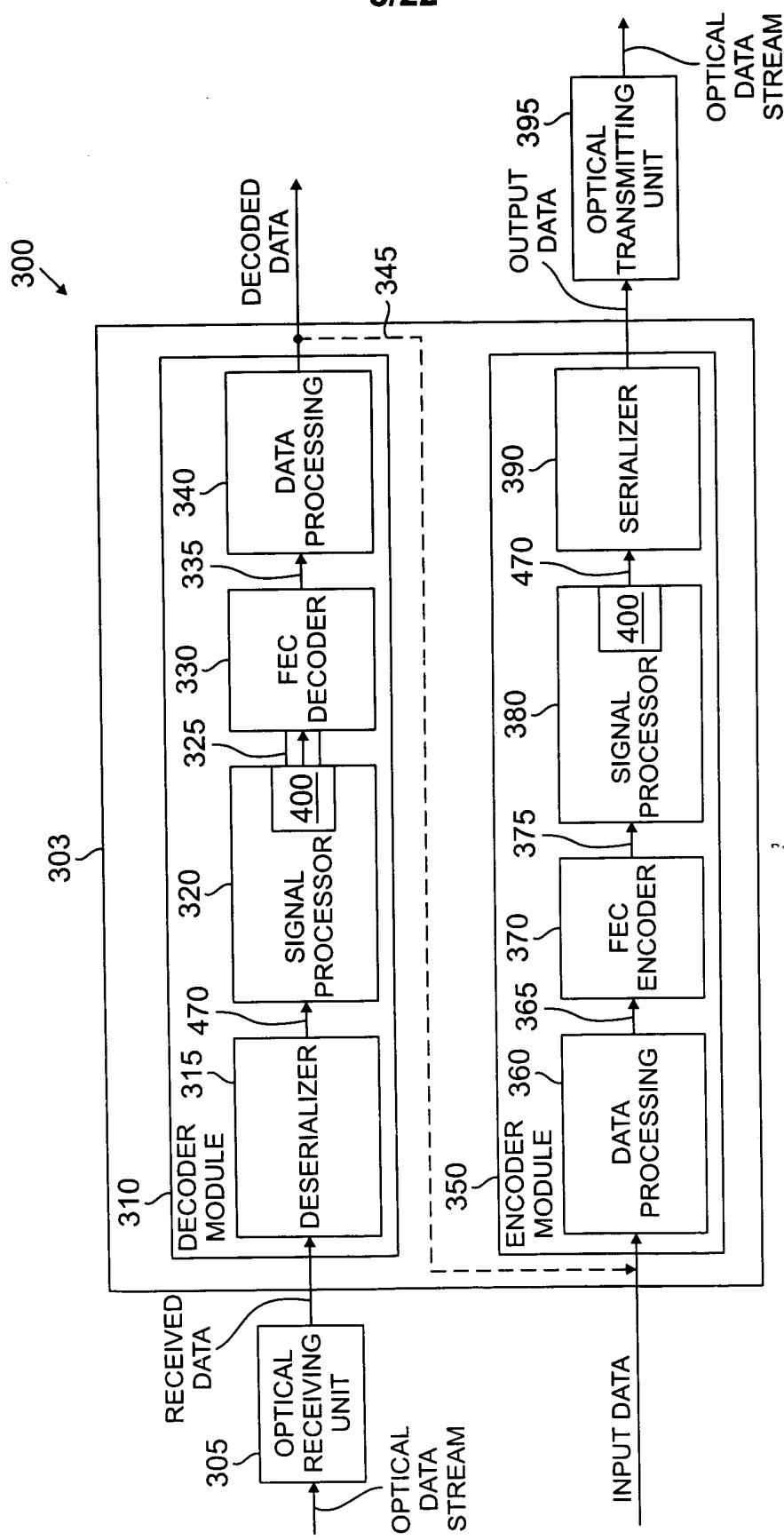


FIG. 2
(PRIOR ART)

**FIG. 3**

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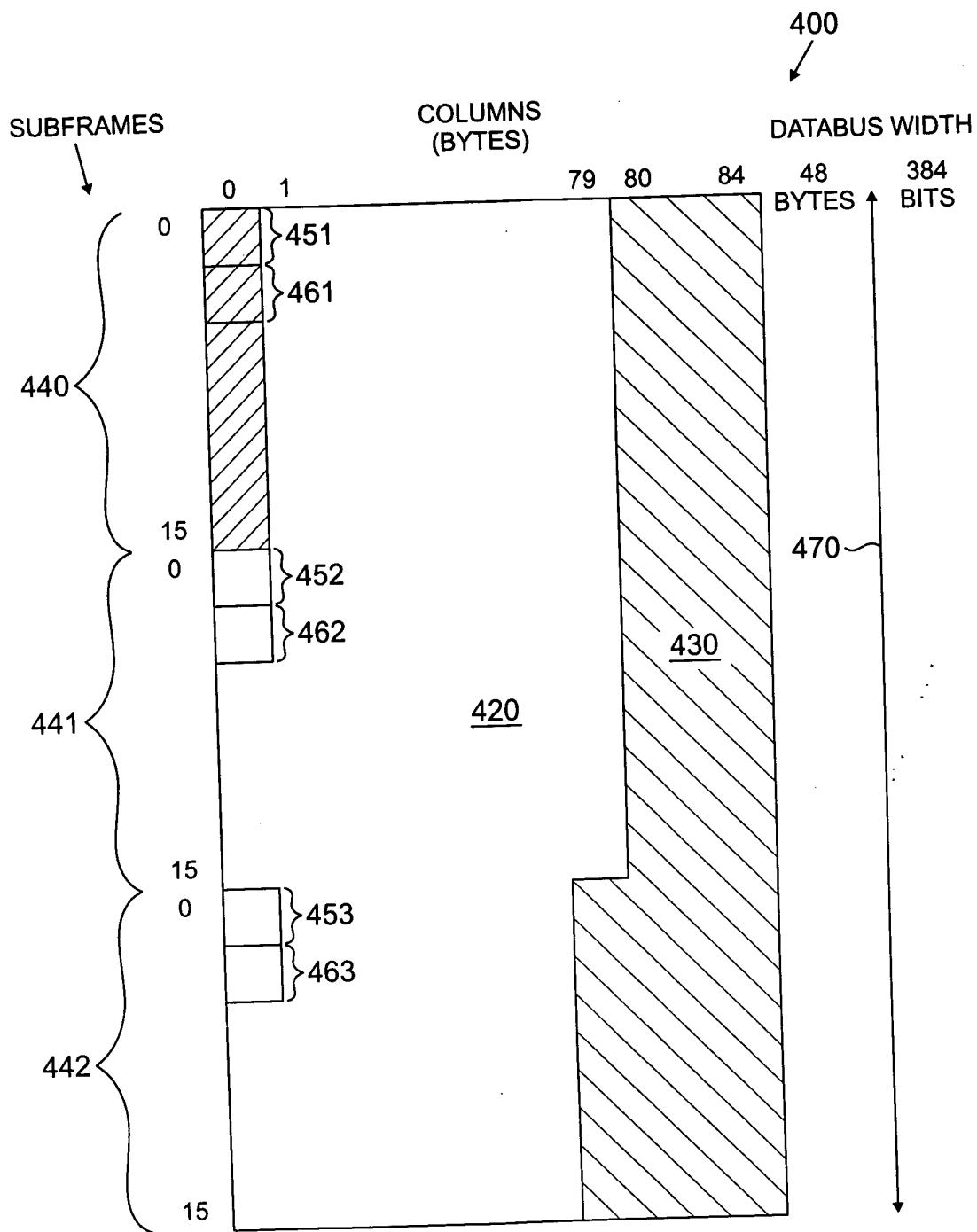


FIG. 4

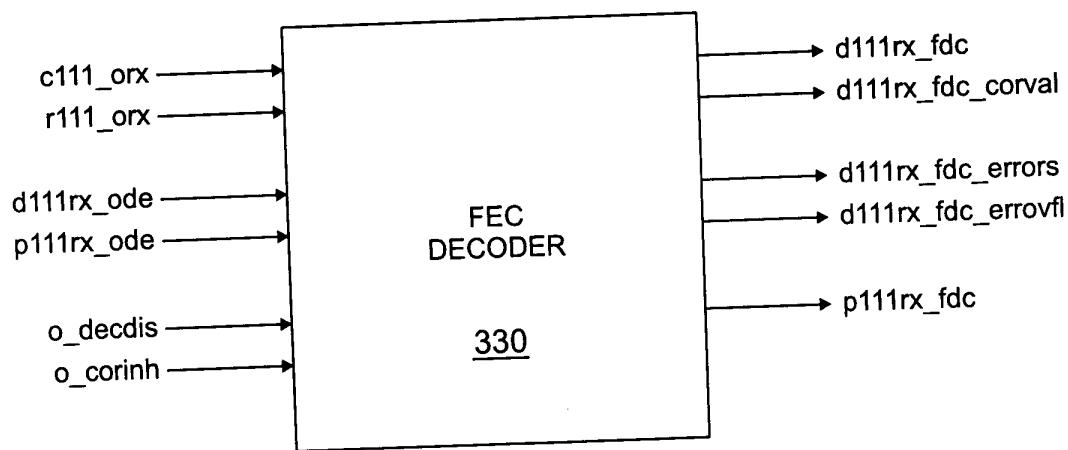


FIG. 5

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NAME	DIRECTION	WIDTH	DESCRIPTION
c111_orx	IN	std_ulogic	SYSTEM CLOCK, 111 MHz
r111_orx	IN	std_ulogic	SIGNAL FOR SYNCHRONOUS RESET OF DECODER
d111rx_ode	IN	(383 DOWN TO 0)	INPUT ENCODED DATA
p111rx_ode	IN	std_ulogic	START OF INPUT FEC BLOCK PULSE
o_decdis	IN	std_ulogic	DECODER FUNCTION ENABLE ('1' = DECODER IS DISABLED)
o_corinh	IN	std_ulogic	ERROR CORRECTION ENABLE ('1' = ERROR CORRECTION INHIBITED)
d111rx_fdc	BUFFER	(383 DOWN TO 0)	OUTPUT DECODED DATA
d111rx_fdc_corval	BUFFER	(383 DOWN TO 0)	OUTPUT CORRECTION VALUES: THIS SIGNAL INDICATES THE BIT POSITION IN THE DATA STREAM d111rx_fdc WHERE A BIT HAS BEEN CORRECTED (VALUES: '0' = NO CORRECTION; '1' = CORRECTION)
p111rx_fdc	BUFFER	std_logic	PULSE INDICATING THE START OF AN OUTPUT FEC BLOCK
d111rx_fdc_errors	BUFFER	(10 DOWN TO 0)	NUMBER OF CORRECTED BIT ERRORS WITHIN ONE FRAME
d111rx_fdc_errorfl	BUFFER	(4 DOWN TO 0)	NUMBER OF UNCORRECTABLE BLOCKS WITHIN ONE FRAME

FIG. 6

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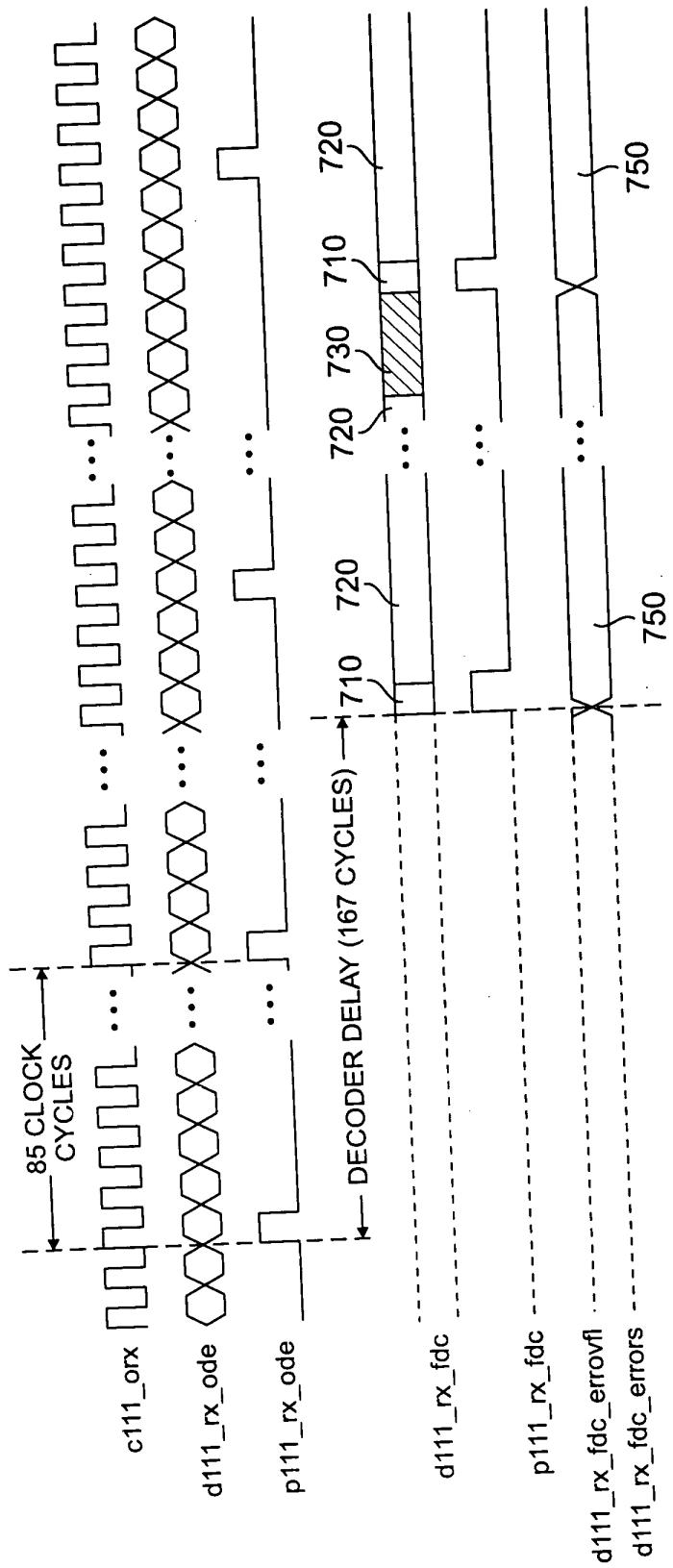


FIG. 7

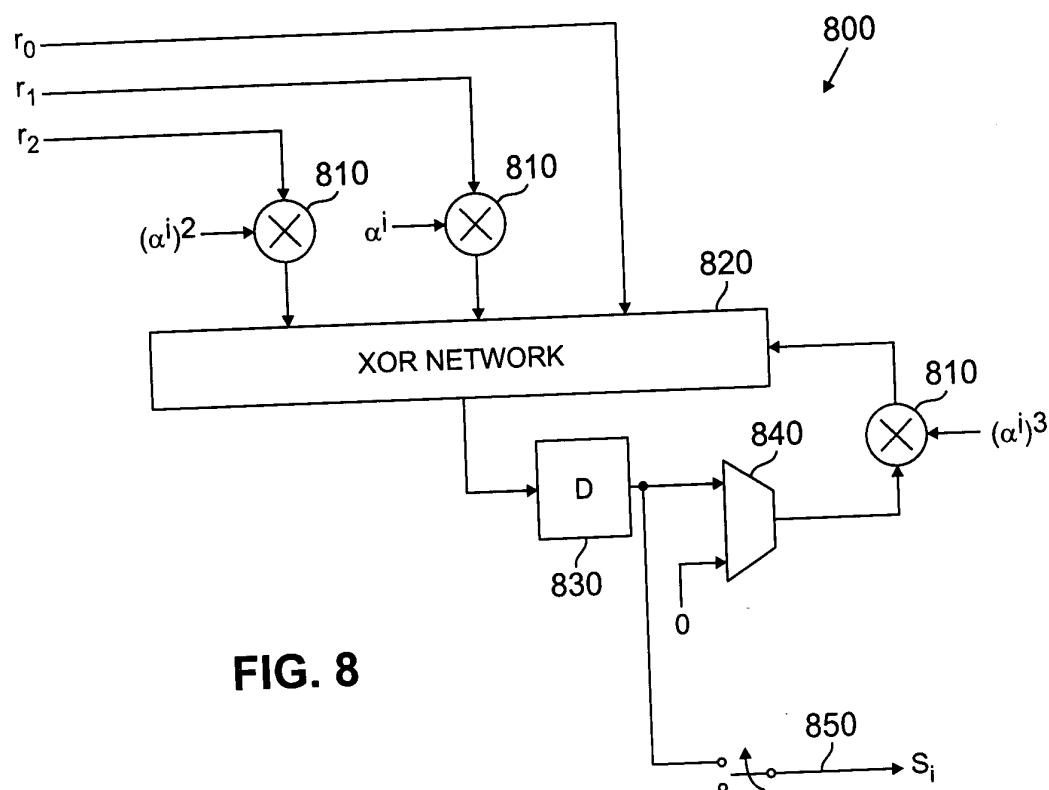


FIG. 8

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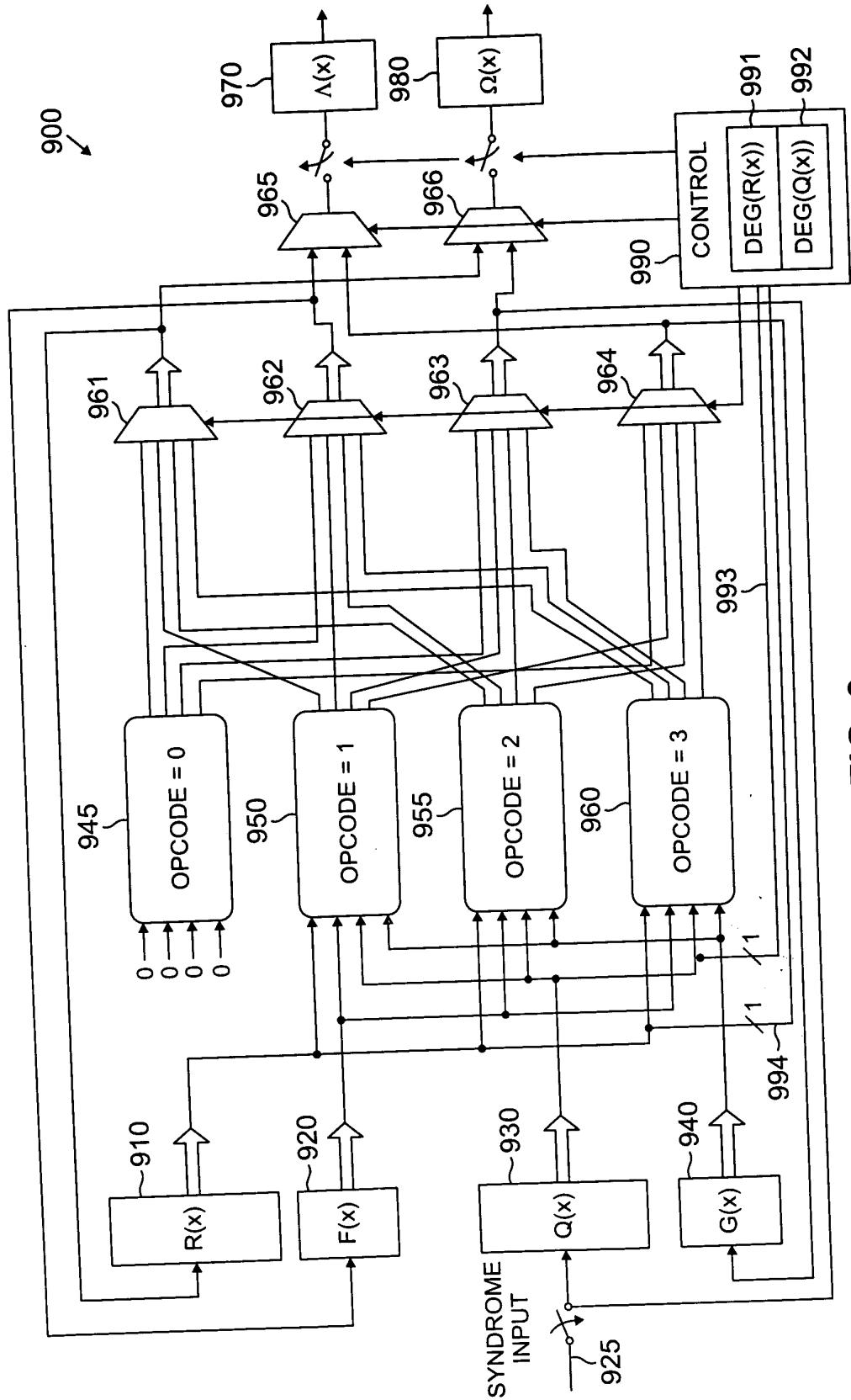
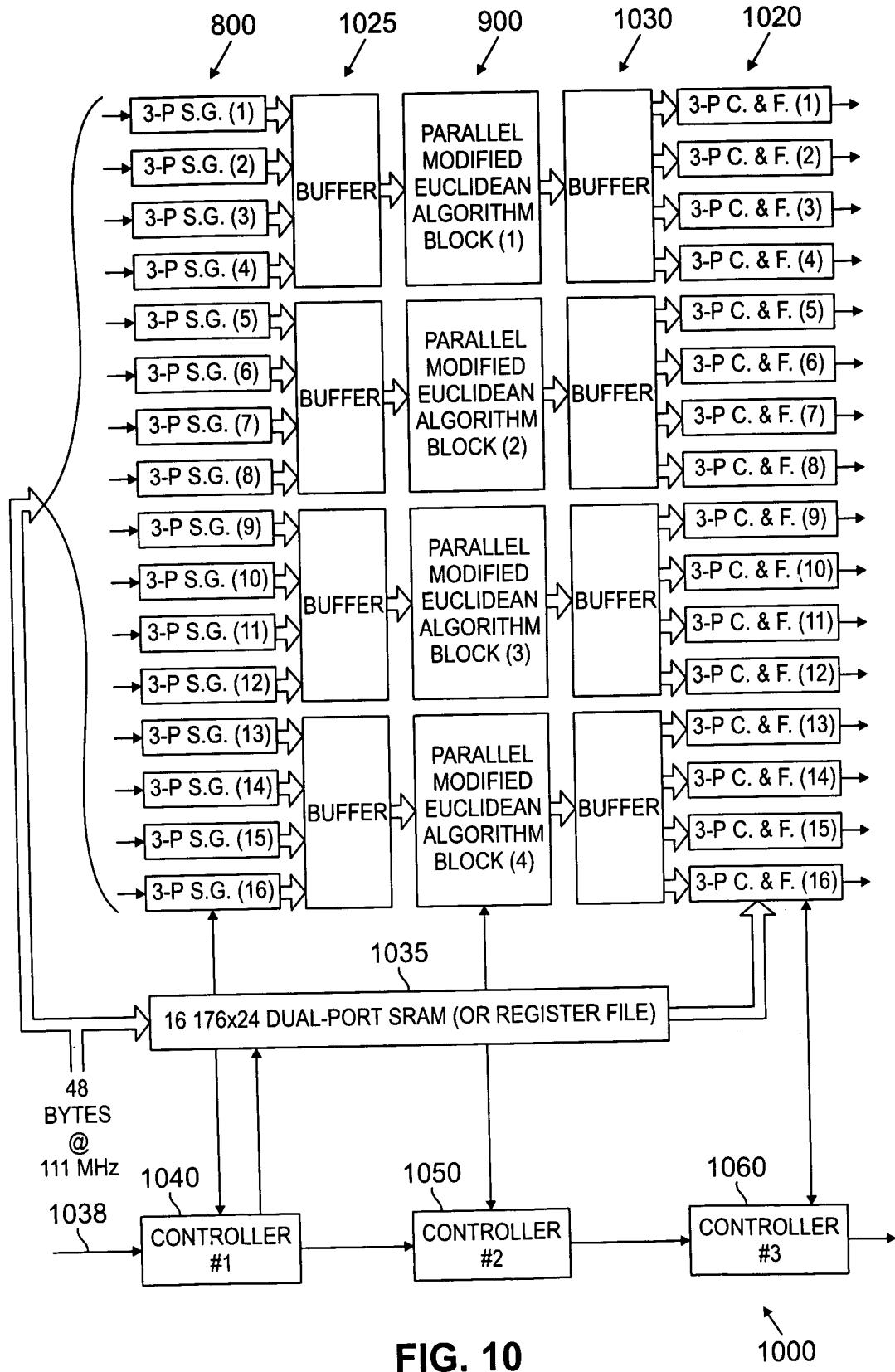
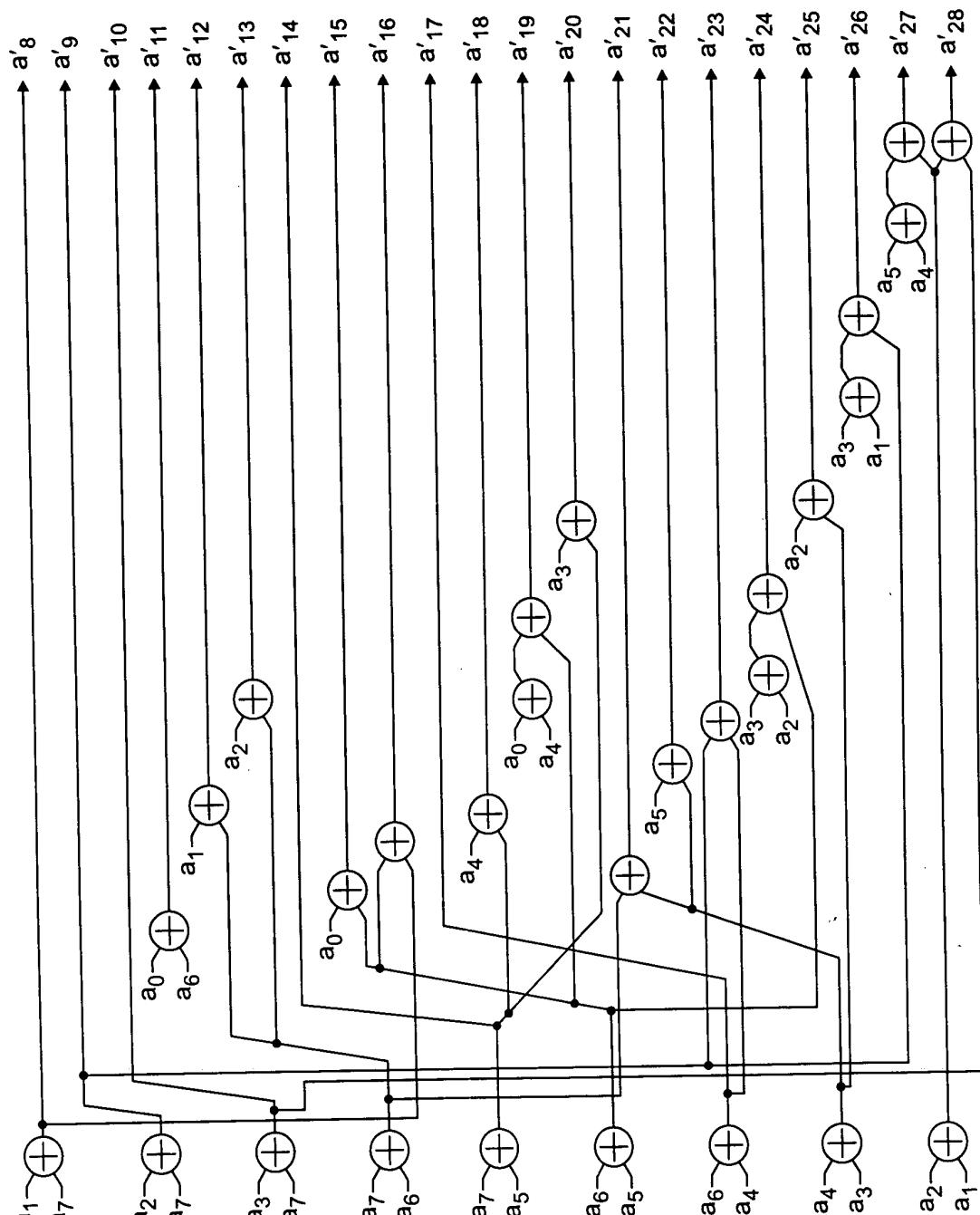


FIG. 9



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1100 →

FIG. 11

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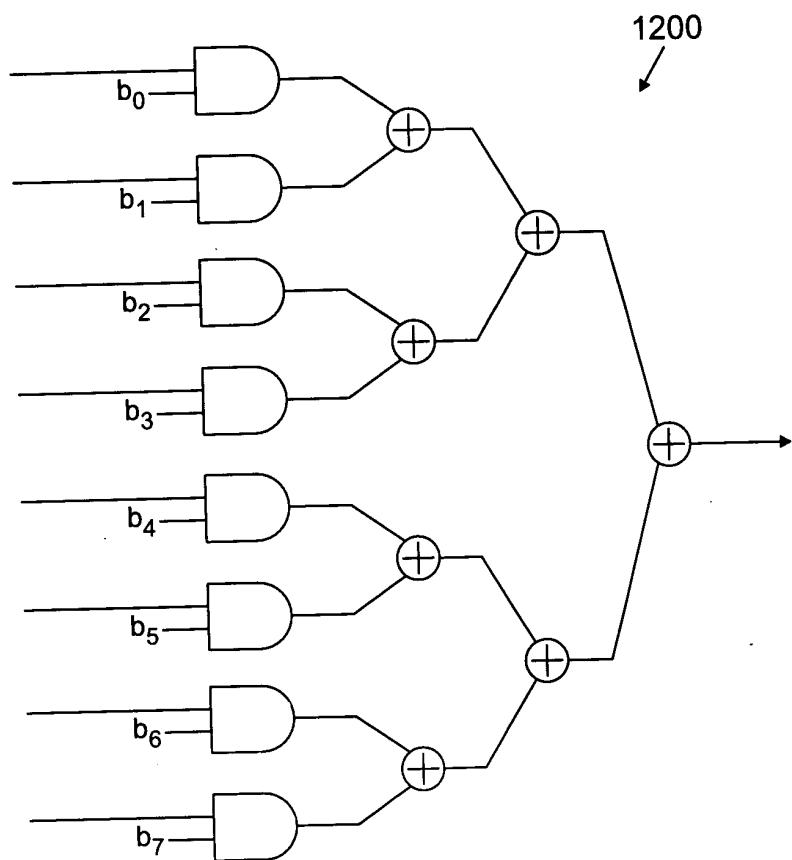


FIG. 12

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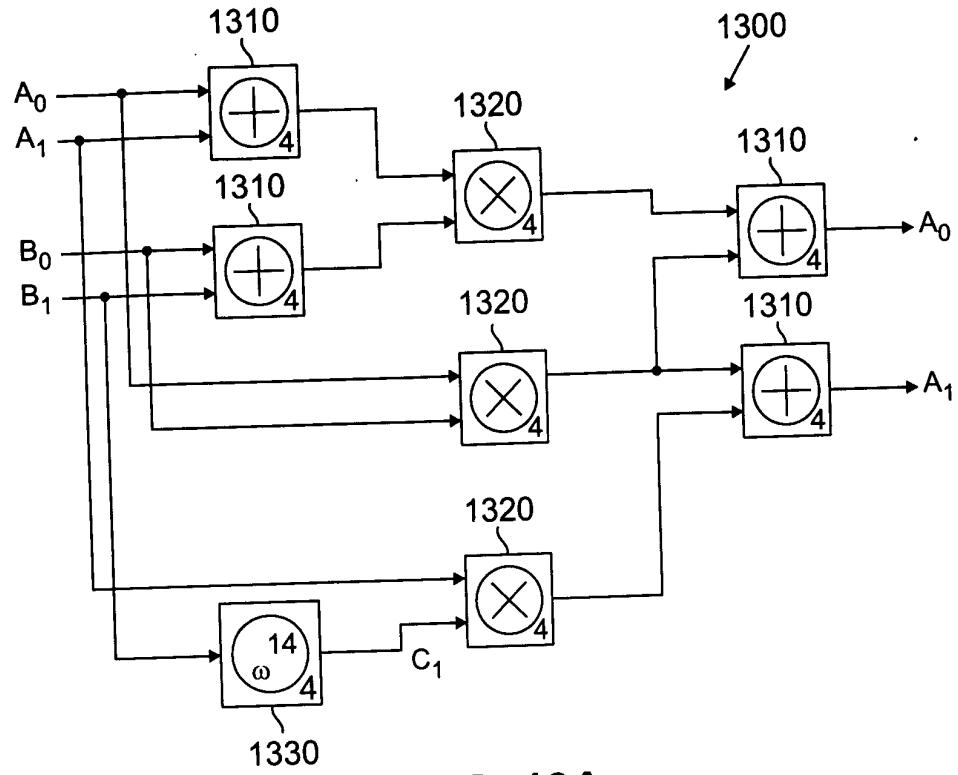


FIG. 13A

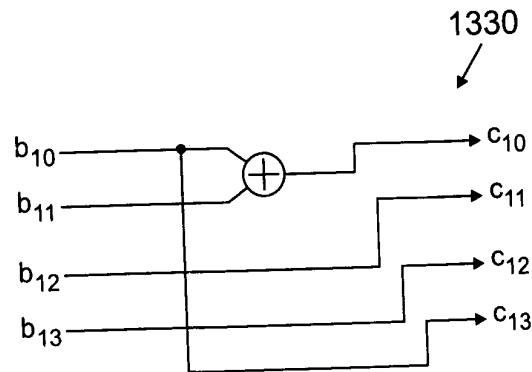


FIG. 13B

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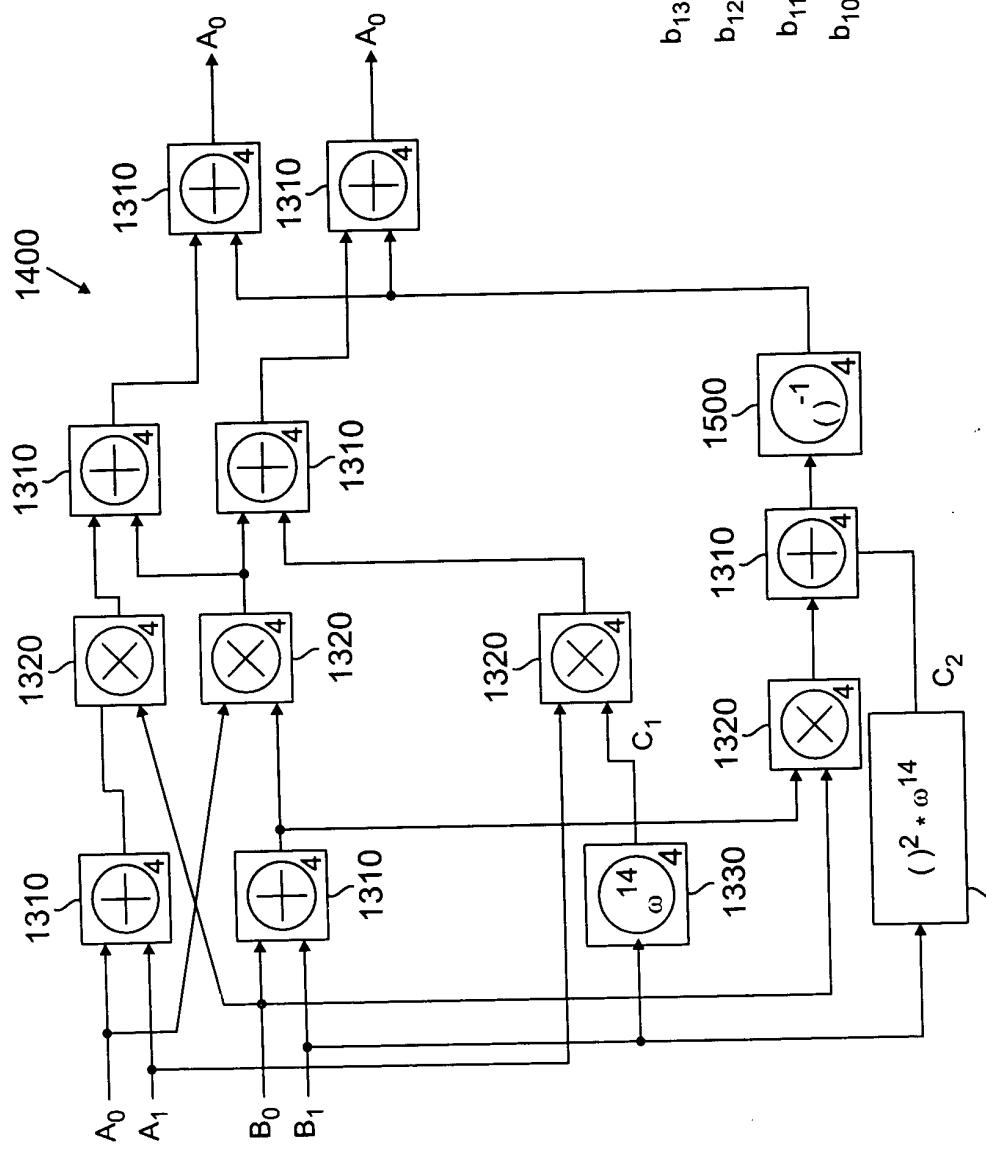


FIG. 14A

FIG. 14B

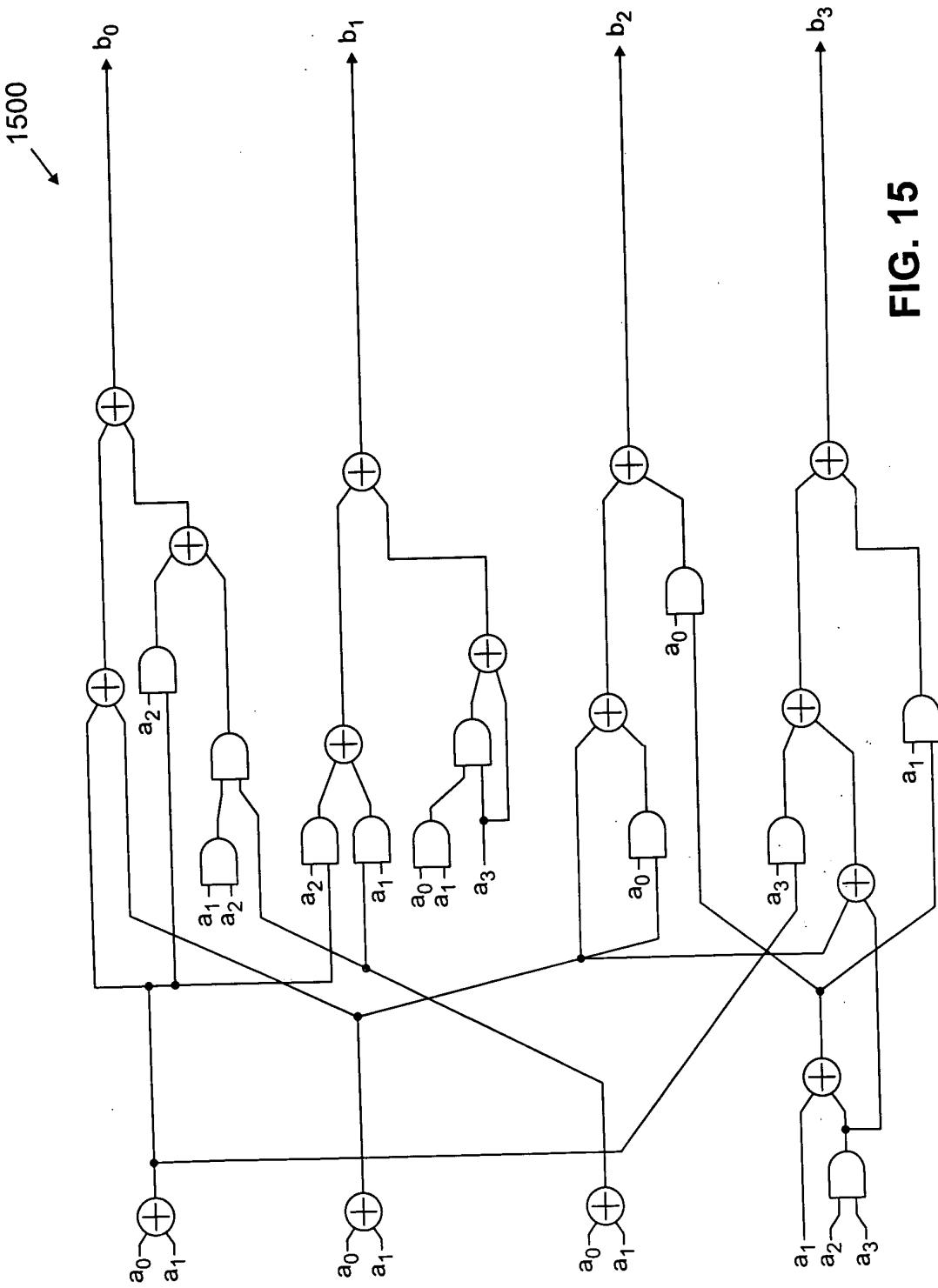


FIG. 15

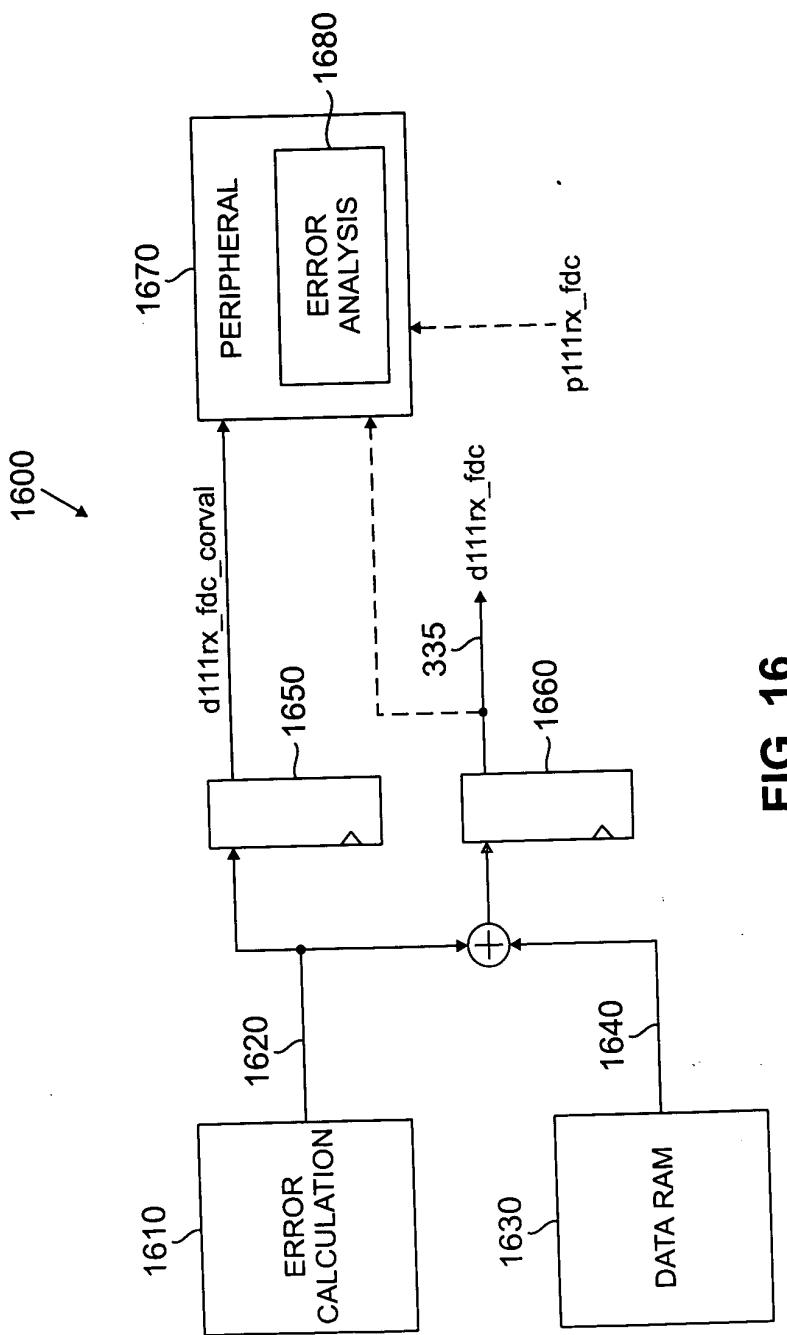


FIG. 16

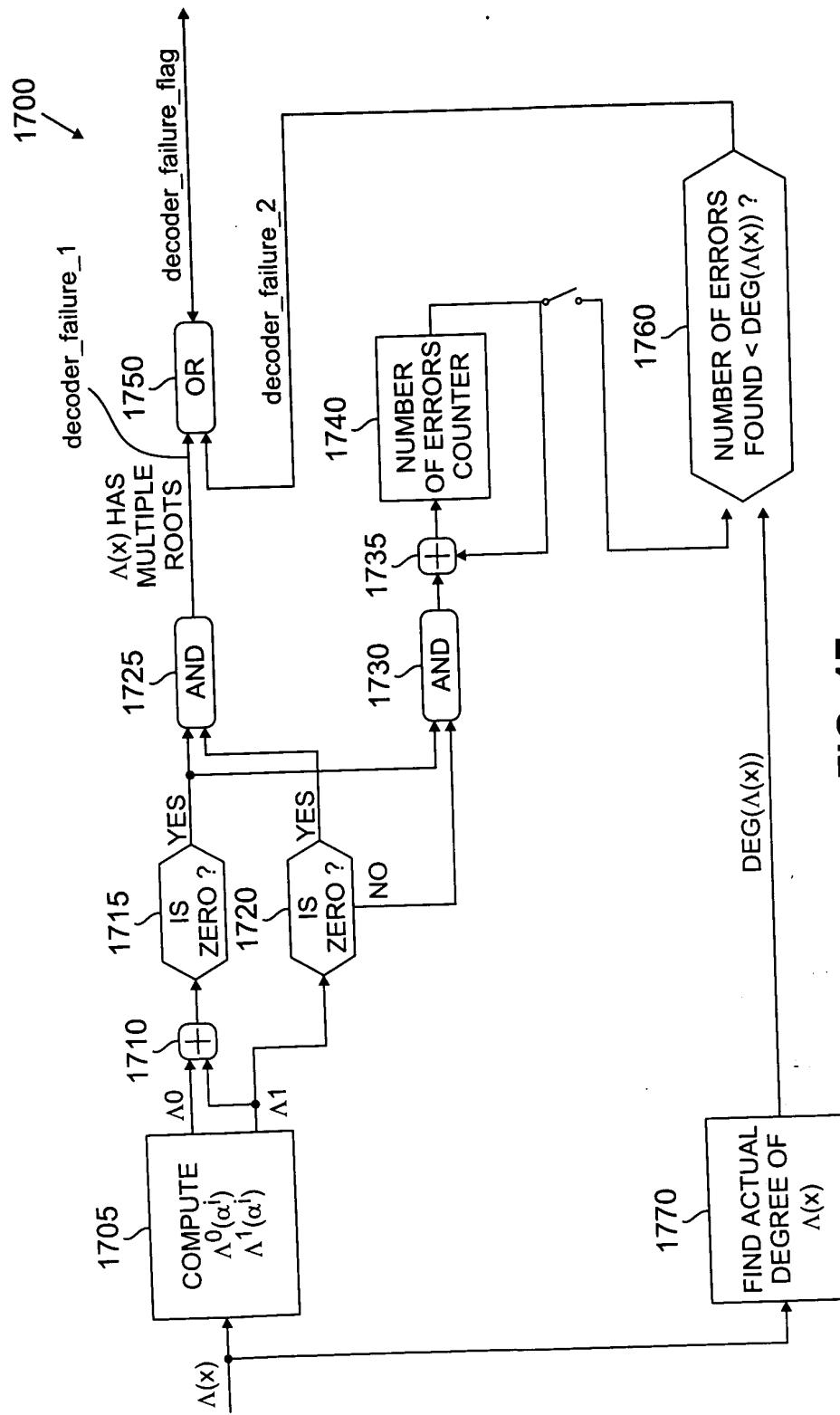


FIG. 17

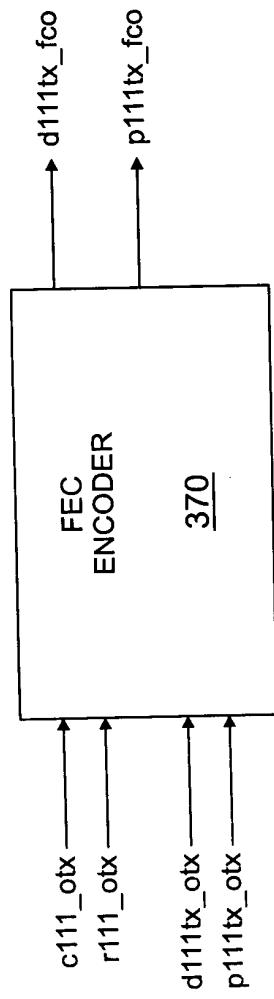
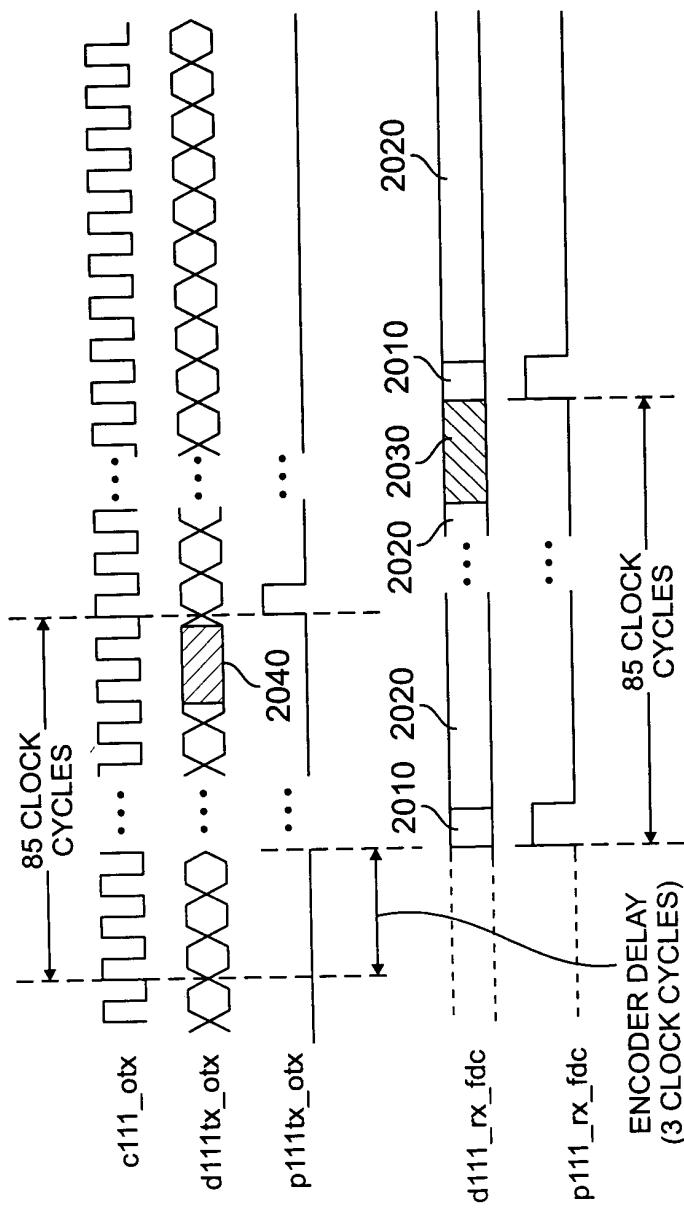
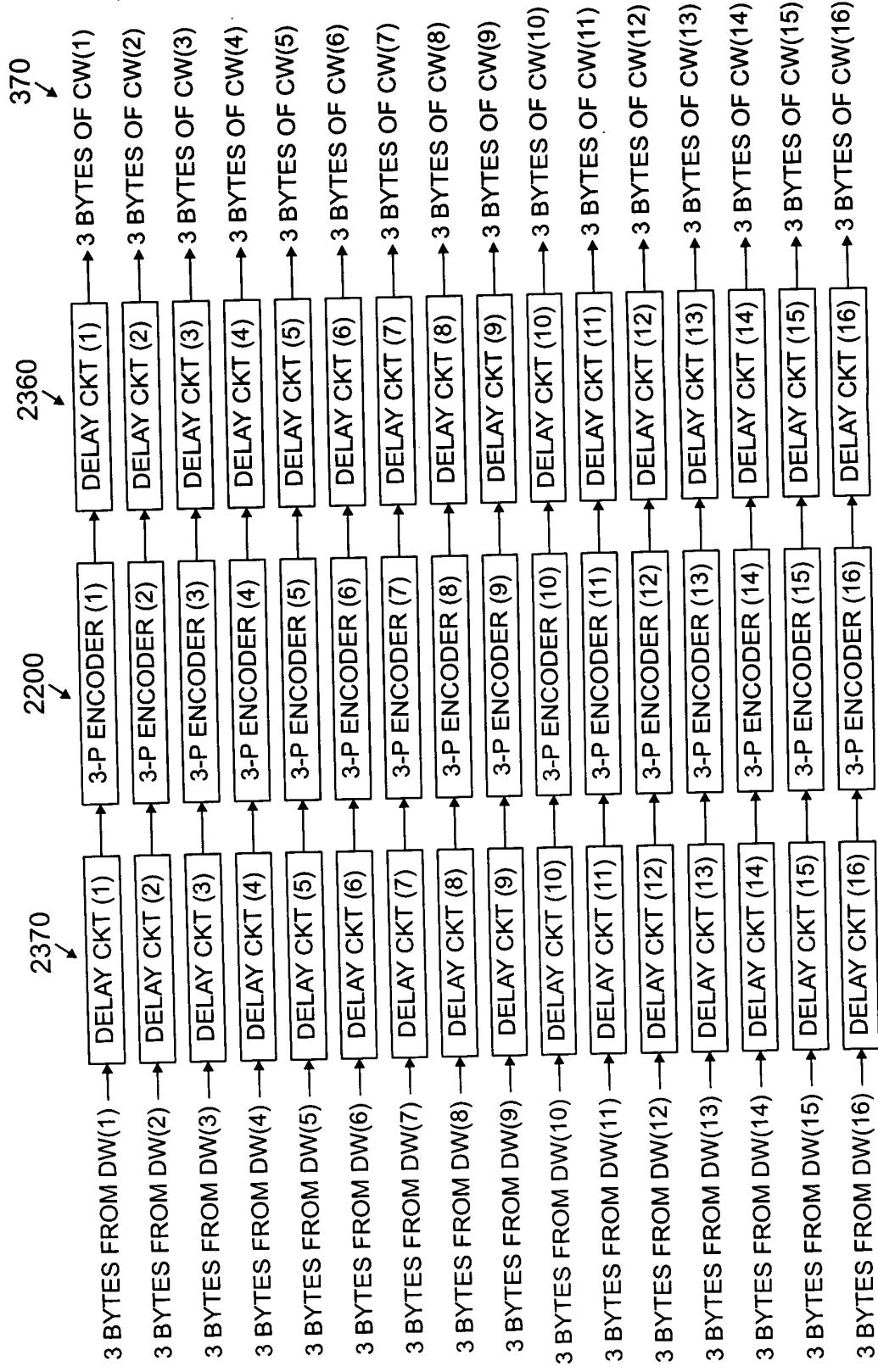


FIG. 18

NAME	DIRECTION	WIDTH	DESCRIPTION
c111_otx	IN	std_ulogic	SYSTEM CLOCK, 111 MHz
r111_otx	IN	std_ulogic	SIGNAL FOR SYNCHRONOUS RESET OF ENCODER
d111tx_otx	IN	(383 DOWN TO 0)	INPUT DATA
p111tx_otx	IN	std_ulogic	START OF INPUT FEC BLOCK PULSE
d111tx_fco	BUFFER	(383 DOWN TO 0)	OUTPUT ENCODED DATA
p111tx_fco	BUFFER	std_ulogic	PULSE INDICATING THE END OF AN FEC BLOCK

FIG. 19

**FIG. 20**

**FIG. 21**

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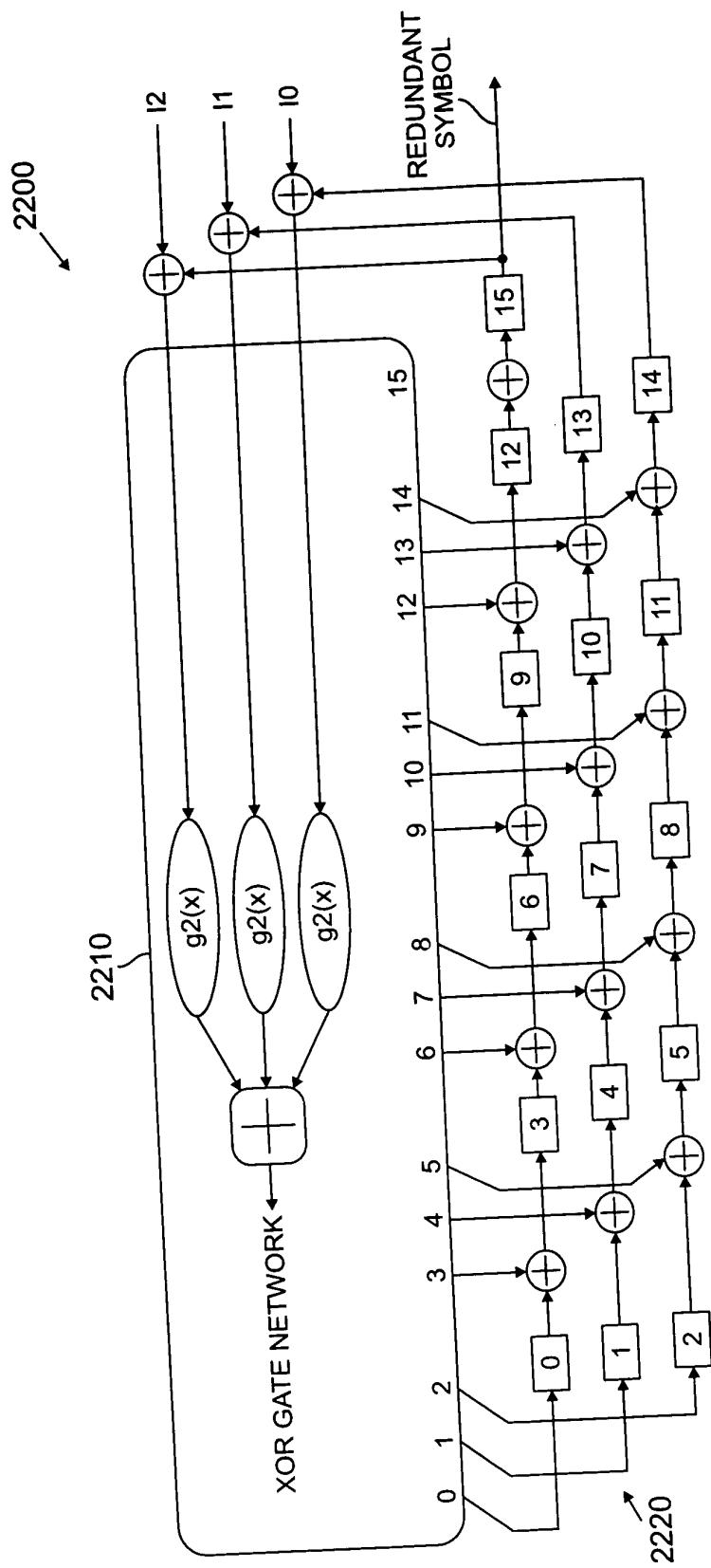


FIG. 22

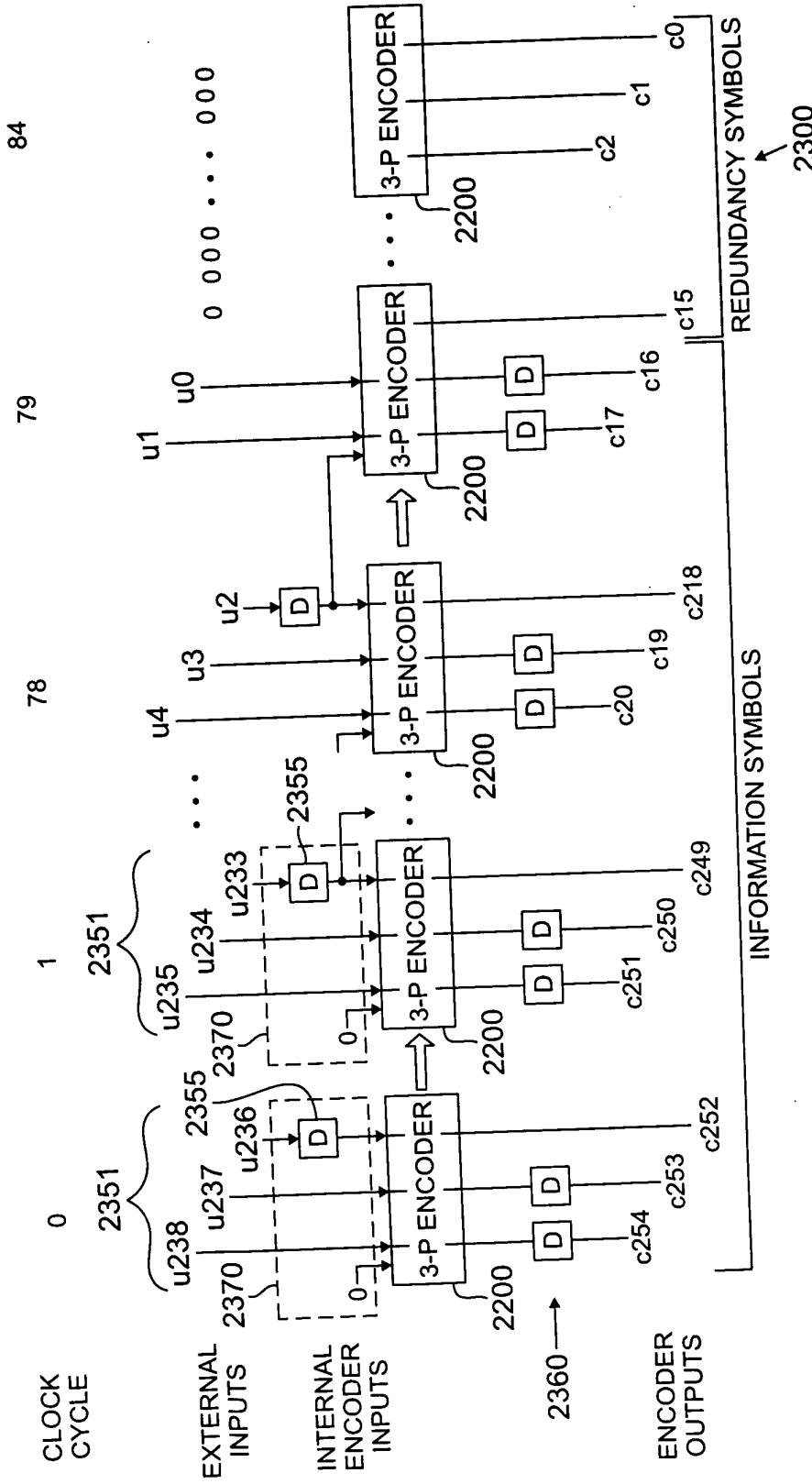


FIG. 23